U.S. Department of Commerce, Patent and Trademark Office	Application No.: 09/802,551
9th SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT BY APPLICANT	Filing date: March 9, 2001
	Inventors: Clive M. Philbrick et al.
	Group Art Unit: 2182
INTELLIGENT NETWORK STORAGE INTERFACE SYSTEM	Examiner name: Unknown
	Attorney Docket No. ALA-012

U.S. Patent Documents

*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date, If Appropriate
JWC	A	5,524,250	6/4/96	Chesson et al.	395	775	
JWC	B	5,619,650	4/8/97	Bach et al.	395	200.01	
JWC	C	5,727,142	3/10/98	Chen	395	181	
JWC	D	5,802,258	9/1/98	Chen	395	182.08	
JWC	E	5,898,713	4/27/99	Melzer et al.	371	53	
JWC	F	6,021,507	2/1/00	Chen	714	2	
JWC	G	6,047,323	4/4/00	Krause	709	227	
	H						

OTHER ART—NON PATENT LITERATURE DOCUMENTS

*Examiner Initial	Cite No.	(Including Author, Title, Date, Pertinent Pages, Etc.)
JWC	1	Schwaderer et al., IEEE Computer Society Press publication entitled, "XTP in VLSI Protocol Decomposition for ASIC Implementation", from 15th Conference on Local Computer Networks, 5 pages, Sept. 30 – Oct. 3, 1990.
JWC	2	Beach, Bob, IEEE Computer Society Press publication entitled, "UltraNet: An Architecture for Gigabit Networking", from 15th Conference on Local Computer Networks, 18 pages, Sept. 30 – Oct. 3, 1990.
JWC	3	Chesson et al., IEEE Syposium Record entitled, "The Protocol Engine Chipset", from Hot Chips III, 16 pages, Aug. 26-27, 1991.
JWC	4	Maclean et al., IEEE Global Telecommunications Conference, Globecom '91, presentation entitled, "An Outboard Processor for High Performance Implementation of Transport Layer Protocols", 7 pages, Dec. 2-5, 1991.
JWC	5	Ross et al., IEEE article entitled "FX1000: A high performance single chip Gigabit Ethernet NIC", from Compcon '97 Proceedings, 7 pages, Feb. 23-26, 1997.
JWC	6	Strayer et al., "Ch. 9: The Protocol Engine" from XTP: The Transfer Protocol, 12 pages, July 1992.
JWC	7	Publication entitled "Protocol Engine Handbook", 44 pages, Oct. 1990.
JWC	8	Koufopavlou et al., IEEE Global Telecommunications Conference, Globecom '92, presentation entitled, "Parallel TCP for High Performance Communication Subsystems", 7 pages, Dec. 6-9, 1992
JWC	9	Lilienkamp et al., Publication entitled "Proposed Host-Front End Protocol", 56 pages, Dec. 1984.

Examiner CMA Date Considered 3/22/06

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with your communication to applicant.

U.S. Department of Commerce, Patent and Trademark Office	Application No.: 09/802,551
SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT BY APPLICANT	Filing date: March 9, 2001
	Inventors: Clive M. Philbrick et al.
	Group Art Unit: 2154
INTELLIGENT NETWORK STORAGE INTERFACE SYSTEM	Examiner name: Chang Jungwon
	Attorney Docket No. ALA-012

U.S. PATENT DOCUMENTS

*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date, If Appropriate
JWC	1	2001/0004354	01/10/01	Jolitz	370	328	—
JWC	2	4,589,063	5/13/86	Shah et al.	710	8	—
JWC	3	5,524,250	6/4/96	Chesson et al.	395	775	—
JWC	4	5,592,622	1/7/97	Isfeld et al.	395	200.02	—
JWC	5	5,619,650	4/8/97	Bach et al.	395	200.01	—
JWC	6	5,727,142	3/10/98	Chen	395	181	—
JWC	7	5,778,013	7/7/98	Jedwab	714	807	—
JWC	8	5,802,258	9/1/98	Chen	395	182.08	—
JWC	9	5,898,713	4/27/99	Melzer et al.	371	53	—
JWC	10	5,970,804	10/26/99	Osborne	395	200.75	—
JWC	11	6,021,507	2/1/00	Chen	714	2	—
JWC	12	6,038,562	3/14/00	Anjur et al.	707	10	—
JWC	13	6,047,323	4/4/00	Krause	709	227	—
JWC	14	6,067,569	5/23/00	Khaki et al.	709	224	—
JWC	15	6,070,200	5/30/00	Gates et al.	710	20	—
JWC	16	6,101,555	8/8/00	Goshey et al.	709	321	—
JWC	17	6,145,017	11/7/00	Ghaffari	710	5	—
JWC	18	6,157,955	12/5/00	Narad et al.	709	228	—
JWC	19	6,172,980	1/9/01	Flanders et al.	370	401	—
	20						
	21						
	22						
	23						
	24						
	25						
	26						
	27						

Examiner [signature] | Date Considered 3/14/06

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with your communication to applicant.

U.S. Department of Commerce, Patent and Trademark Office	Application No.: 09/802,551
10th SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT BY APPLICANT	Filing date: March 9, 2001
	Inventors: Clive M. Philbrick et al.
	Group Art Unit: 2154
INTELLIGENT NETWORK STORAGE INTERFACE SYSTEM	Examiner name: Chang Jungwon
	Attorney Docket No. ALA-012

OTHER ART—NON PATENT LITERATURE DOCUMENTS

*Examiner Initial		(Including Author, Title, Date, Pertinent Pages, Etc.)
JWC	1	Beach, Bob, IEEE Computer Society Press publication entitled, "UltraNet: An Architecture for Gigabit Networking", from 15th Conference on Local Computer Networks, 18 pages, Sept. 30 – Oct. 3, 1990.
JWC	2	Chesson et al., IEEE Syposium Record entitled, "The Protocol Engine Chipset", from Hot Chips III, 16 pages, Aug. 26-27, 1991.
JWC	3	Intel article entitled "Solving Server Bottlenecks with Intel Server Adapters", Copyright Intel Corporation, 1999, 8 pages.
JWC	4	Koufopavlou et al., IEEE Global Telecommunications Conference, Globecom '92, presentation entitled, "Parallel TCP for High Performance Communication Subsystems", 7 pages, Dec. 6-9, 1992.
JWC	5	Lilienkamp et al., Publication entitled "Proposed Host-Front End Protocol", 56 pages, Dec. 1984.
JWC	6	Maclean et al., IEEE Global Telecommunications Conference, Globecom '91, presentation entitled, "An Outboard Processor for High Performance Implementation of Transport Layer Protocols", 7 pages, Dec. 2-5, 1991.
JWC	7	Publication entitled "Protocol Engine Handbook", 44 pages, Oct. 1990.
JWC	8	Ross et al., IEEE article entitled "FX1000: A high performance single chip Gigabit Ethernet NIC", from Compcon '97 Proceedings, 7 pages, Feb. 23-26, 1997.
JWC	9	Schwaderer et al., IEEE Computer Society Press publication entitled, "XTP in VLSI Protocol Decomposition for ASIC Implementation", from 15th Conference on Local Computer Networks, 5 pages, Sept. 30 – Oct. 3, 1990.
JWC	10	Strayer et al., "Ch. 9: The Protocol Engine" from XTP: The Transfer Protocol, 12 pages, July 1992.
JWC	11	Thia, Y.H. Publication entitled "High-Speed OSI Protocol Bypass Algorithm with Window Flow Control", Protocols for High Speed Networks, pages 53-68, 1993.
JWC	12	Thia, Y.H. Publication entitled " A Reduced Operational Protocol Engine (ROPE) for a multiple-layer bypass architecture", Protocols for High Speed Networks, pages 224-239, 1995.
JWC	13	WindRiver article entitled "Tornado: For Intelligent Network Acceleration", copyright Wind River Systems, 2001, 2 pages.
JWC	14	WindRiver White Paper entitled "Complete TCP/IP Offload for High-Speed Ethernet Networks", Copyright Wind River Systems, 2002, 7 pages.

Examiner	CMG Jwm	Date Considered	3/14/06

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with your communication to applicant.